

1.

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):

Douglas D. Coolbaugh, et al. Examiner:

Unassigned

Serial No: 10/605,439Filed: 9/30/03

**Art Unit:** 

Unassigned

**Docket:** BUR920020094US1 (16895)

For: PRECISION POLYSILICON

Dated: ////3/03

**RESISTOR PROCESS** 

Commissioner for Patents United States Patent Office Alexandria, VA 23313-1450

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

- Japanese Patent Publication No. JP5275619, dated October 22, 1993;
- 2. C.H. Lee, IBM Disclosure Bulletin "Polysilicon Resistors Compatible with Bipolar Integrated Circuits ad Method of Manufacture", Vol. 25, No. 5, October 1982; and
- 3. G.R. Goth, et al., IBM Disclosure Bulletin "Planar Self-Aligned Metal/Sidewall and Polysilicon-Resistor Process", Vol. 25, No. 2, July 1982.

## CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Box 1450, Alexandria, VA 22313-1450 on

G:\Ibm\1126\16895\Amend\SUPPIDS.doc

Applicants are submitting copies of the above-cited references.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,

Leslie S. Szívos, Ph.D. Registration No.: 39,394

Scully, Scott, Murphy & Presser 400 Garden City Plaza Garden City, New York 11530 (516) 742-4343

Enclosure

PTO 1449

Three (3) references

| Form PTO-1449 U.S. DEPARTMENT OF COMMERCE (REV. 7-80)PATENT AND TRADEMARK OFFICE  LIST OF PRIOR ART |       |   |                | Atty. Docket N .<br>BUR920020094US1 (16895) |                            | Serial N .    |             |               |
|---|-------|---|----------------|---|----------------------------|---------------|-------------|---------------|
|   |       | NOV '   | 1 7 2003       | Applicant Douglas D. Coolbaug               | gh, et al.                 |               |             |               |
| (Use several sheets if necessary)  (Use several sheets if necessary)                                |       |   |                | Filing Date                                 | <b>Group</b><br>Unassigned |               |             |               |
| U.S. PAT  | ENT [ | OCUMENTS  |                |   |                            |               |             |               |
| EXAMINER INITIAL*   |       | DOCUMENT NUMBER   | DATE           | NAME  | CLASS                      | SUBCLASS      | _           | DATE opriate) |
|   | AA    |   |                |   |                            |               |             |               |
| ·   | AB    |   | <u>.</u>       |   |                            |               |             |               |
|   |       |   | ·              |   |                            |               |             |               |
|   |       |   |                |   |                            |               |             |               |
|   |       |   |                |   |                            |               |             |               |
|   |       |   |                |   |                            |               |             |               |
|   |       |   |                |   |                            |               |             |               |
|   |       |   |                |   |                            |               |             | <del></del>   |
|   |       |   |                |   |                            |               |             |               |
| FOREIGN   | N PAT | ENT DOCUMENTS   |                |   |                            |               |             |               |
|   |       | DOCUMENT NUMBER   | DATE           | COUNTRY                                     | CLASS                      | SUBCLASS      | TRANSLATION |               |
|   |       |   |                |   |                            |               | YES         | МО            |
| 1989-19   |       | JP5275619   | 10/22/1993     | 3 JAPAN                                     |                            |               |             |               |
| OTHER R   |       | DT (I al. di a  | 1 D : D ::     |   |                            |               |             |               |
| OTHER PI  | NOK A | RT (Including Author, Ti  |                |   | s Compatible               | e with Bipola | r Integra   | nted          |
|   |       | C.H. Lee, IBM Disclosure Bulletin "Polysilicon Resistors Compatible with Bipolar Integrated Circuits ad Method of Manufacture", Vol. 25, No. 5, October 1982; and |                |   |                            |               |             |               |
|   |       | G.R. Goth, et al., IBM Disclosure Bulletin "Planar Self-Aligned Metal/Sidewall and Polysilicon-Resistor Process", Vol. 25, No. 2, July 1982.                      |                |   |                            |               |             |               |
|   |       | Resistor Process", V  | ol. 25, No. 2, | July 1982.                                  |                            | ·····         |             |               |
|   |       |   |                |   |                            |               |             |               |
|   |       |   |                |   |                            |               |             |               |
|   | 1_    |   |                |   |                            |               |             |               |